AMENDMENTS TO THE CLAIMS

Please amend Claims 1, 2, 4, 6, 7, 9-11, 13, 14, and 16-20 of the Application as follows, and cancel Claim 8 of the Application, without prejudice or disclaimer to continued examination on the merits:

1. (Currently Amended): A circuit comprising:

an array of cells comprising at least a current cell and a previous cell operably connected according to a sequence, ~~each of the cells including~~ at least the current cell comprising:

a first multiplexer, ~~said~~ the first multiplexer receiving a plurality of ~~first bit~~ data streams,

a space control register coupled to control the first multiplexer, ~~and~~

a latch coupled to receive a ~~signal~~ selected data stream from the plurality of data streams from the first multiplexer~~; and~~,

a second multiplexer, the second multiplexer selectively receiving a selected bit from the selected data stream from the latch and a data stream from the previous cell, and

a control logic coupled to control the second multiplexer; and

a control circuit coupled to control the latch of ~~each of the cells~~ at least the current cell to select ~~one or more bits from a stream of bits output by the multiplexer of each of the cells~~ the selected bit from the selected data stream~~, wherein~~

~~at least one cell in the sequence is coupled to a previous cell in the sequence in order to receive one or more bits output by the previous cell~~.

2. (Currently Amended): The circuit of claim 1 wherein the first multiplexer comprises a plurality of multiplexers.

3. (Original): The circuit of claim 2 wherein the plurality of multiplexers comprise first, second, third, fourth, and fifth multiplexers.

4. (Currently Amended): The circuit of claim 3 wherein the first, second, third, and fourth multiplexers ~~are~~ comprise 8:1 multiplexers.

5. (Original): The circuit of claim 3 wherein the fifth multiplexer comprises a 6:1 multiplexer coupled to receive an output from the first multiplexer, an output from the second multiplexer, an output from the third multiplexer, an output from the fourth multiplexer, a logical "one", and a logical "zero".

6. (Currently Amended): The circuit of claim 1 wherein the space control register programmably stores a value indicating ~~a selected bit from a plurality of bits~~ the selected data stream from the plurality of data streams.

7. (Currently Amended): The circuit of claim 1 wherein the control circuit comprises:

a time control register to store a value indicating a the selected bit from ~~a sequence of bits~~ the selected data stream;

a counter to count bits in the ~~sequence of bits~~ selected data stream from a predetermined bit; and

a comparator coupled to the time control register and to the counter to generate a load signal when ~~a~~ the value stored in the time control register and a value provided by the counter are equal, the load signal to cause the latch of ~~a~~ the current cell in the sequence to load a value output by the first multiplexer of ~~that~~ the current cell.

8. (Canceled)

9. (Currently Amended): The circuit of claim ~~8~~ 1 further comprising ~~a second~~ an additional latch in ~~the~~ at least ~~one~~ the current cell configured to receive a signal output by the second multiplexer.

10. (Currently Amended): The circuit of claim 1~~,~~ wherein the first multiplexer receives logical values to generate alarm signals.

11. (Currently Amended): A method in a cell, which is implemented in an array of cells operably connected according to a sequence, the method comprising:

receiving multiple first streams of bits at a first multiplexer in the ~~implemented~~ cell;

selecting one or more bits from one of ~~said~~ the received multiple first streams of bits to be latched within the ~~implemented~~ cell based, at least in part, on a space control register value and a time control register value;

receiving at a second multiplexer in the ~~implemented~~ cell one or more bits output by a previous cell in the sequence; and

outputting a second stream of bits including ~~said~~ the selected one or more bits and the one or more bits received from the previous cell.

12. (Original): The method of claim 11 wherein the space control register indicates a selected stream of data from a plurality of streams of data.

13. (Currently Amended): The method of claim 12~~,~~ wherein the space control register is programmable.

14. (Currently Amended): The method of claim 11~~,~~ wherein the time control register indicates one or more bits from a selected stream of data.

15. (Currently Amended): The method of claim 14~~,~~ wherein the time control register is programmable.

16. (Currently Amended): The circuit of claim 1~~,~~ wherein ~~the~~ at least ~~one of the cells~~ the current cell is configured to:

output ~~the~~ one or more bits from the previous cell during an interval in which no bits are selected by the ~~at least one~~ current cell's latch, and

output ~~the~~ one or more selected bits during an interval in which the ~~at least one~~ current cell's latch selects the one or more selected bits.

17. (Currently Amended): The circuit of claim 1~~,~~ wherein

~~the~~ a first stream of bits output by the first multiplexer of the ~~at least one~~ current cell conforms to a first format, and

the ~~at least one~~ current cell outputs ~~the~~ one or more selected bits in such a manner as to output a second ~~bit~~ stream of bits corresponding to a second format.

18. (Currently Amended): The method of claim 11~~,~~ wherein ~~the~~ outputting the second stream of bits ~~includes~~ comprises:

outputting the one or more bits received from the previous cell during an interval in which no bits are latched by the ~~implemented~~ cell.

19. (Currently Amended): The method of claim 18~~,~~ wherein ~~the~~ outputting the second stream of bits ~~includes~~ comprises:

outputting the one or more selected bits during an interval in which the ~~implemented~~ cell latches the one or more selected bits.

20. (Currently Amended): The method of claim 11~~,~~ wherein

the one of ~~said~~ the received multiple first streams of bits conforms to a first format, and

the ~~implemented~~ cell outputs the second stream of bits such that the second stream of bits conforms to a second format.